# High Performance Flip-Chip Multi-Mode, Multi-Band VCO IC Using A Standard Low Cost BiCMOS Process

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**Abstract- A low cost, high performance flip-chip multi-mode, multi-band voltage controlled oscillator (VCO) IC is presented. This IC is suitable for high performance VCO circuits over a wide range of frequencies. A novel noise reduction circuit technique is used to obtain improved phase noise performance without the use of a higher cost SiGe BiCMOS processes. This IC has a measured phase noise of -162dBc/Hz at a 20MHz offset operating at an oscillation frequency of 900MHz with an output power of +10dBm.**

## I. INTRODUCTION

VCOs are an integral part of all modern communications systems. In many of today's cellular telephony applications, a low cost high performance VCO is called upon to work at many different frequencies for standards such as TDMA, CDMA and GSM. As of the time of this paper, these communications standards require the use of external resonators to achieve the required oscillator phase noise performance. Hence, these oscillators are often constructed in modules that are manufactured to a single cellular frequency range and mode. Until recently this required the use of multiple VCO modules in the multi-mode phones that are manufactured.

This paper describes a very flexible IC that can be used with external tank circuits to provide two separate oscillators with different frequency ranges, provisions for frequency "band switching" with external PIN diodes, and includes up to three individually controlled output buffers to drive external circuits.

## II. TECHNOLOGY

The VCO IC was constructed on one of Motorola's low cost 8-inch BiCMOS process with the following attributes [1]:

- NMOS, Isolated NMOS and PMOS Devices
- High $V_T$, Low $V_T$ and Native MOS Devices
- 0.4µm Minimum Drawn MOS Gate Length
- Vertical NPN and Lateral PNP
- 0.4µm Minimum Drawn BJT Emitter Width
- 25 GHz NPN Peak $f_\tau$ (0.8µm x 0.4µm BJT)
- Double-Poly Capacitors (4fF/µm$^2$)
- High Q Cu Inductors
- Poly Resistors (High and Low Sheet ρ)
- Trench Isolation
- "Sinker" Substrate Contacts
- Three Metal Layers

It was determined that a lower cost 0.4µm BiCMOS process could provide the performance required with some novel circuit techniques. It should be noted that this version of the IC process does not include metal-insulator-metal (MIM) capacitors or SiGe BJT devices.

Flip-chip technology is used to attach the die to the external components of the VCO and output buffer matching networks. This technology allows the IC to be mounted directly to a circuit board removing the package parasitics which cause significant difficulty in high frequency designs. Flip chip die attach also reduces the physical dimensions of the VCO by eliminating the space required for the package.

The final die size is 1.0mm x 2.1mm with "staggered" rows of 5mil diameter solder bumps that have a pitch of 0.42mm. A plot of the die layout is shown in Figure 1.

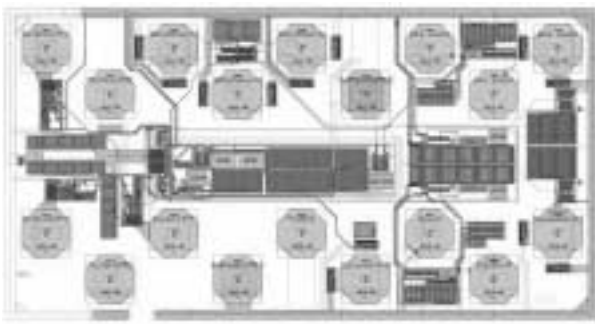

Figure 1. VCO IC die plot.

## III. FUNCTIONAL DESCRIPTION

A top level diagram of the major circuit blocks of the VCO IC is shown in Figure 2. The VCO IC has the following functional blocks:

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- Two common collector Colpitts oscillators with externally programmable bias
- Three independently enabled output buffers with externally programmable bias
- Two PIN diode drivers for oscillator tank circuit band switching
- CMOS logic compatible enable control inputs

Some of the functional features of this IC are:

- Power supply independent operation over a supply voltage range of 2.25V to 3.0V
- Output buffers can be disabled with logic input or by removing the supply voltage from the output pin
- Buffer outputs can be combined for additional output power
- Externally programmable oscillator for optimum oscillator operating point
- Externally programmable buffer bias for customizing the output power delivered by the buffers.

It is evident from the functional description of the VCO IC, that this IC to can be adapted many different applications and environments.

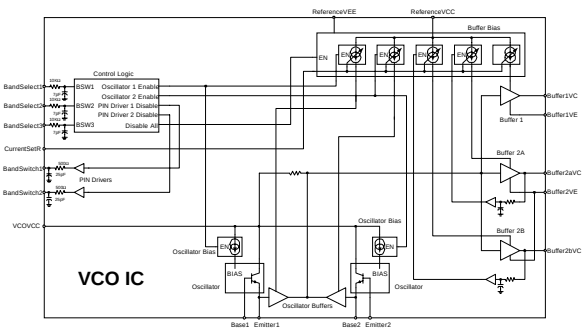


Figure 2. Top level diagram of the VCO IC.

## IV. BLOCK DESCRIPTION

A top level block diagram of the VCO IC is shown in Figure 2.

### A. Control Logic

The VCO IC control logic is implemented with standard CMOS logic gates. These gates decode the input signals into enable and disable the oscillators, output buffers and the external PIN diodes.

### B. PIN Drivers

The PIN Drivers are CMOS outputs capable of driving PIN diodes that are used to “band switch” the tank circuit a VCO. These drivers also include an internal current limiting resistor and are capable of driving a PIN diode with up to 5mA of current.

### C. Buffer Bias

The Buffer Bias contains current regulators which are enabled and disabled by the Control Logic to provide supply independent current to the output buffers. This cell also receives another enable control signal derived from the presence or absence of a supply voltage to the output buffers. An external resistor can be used to set the bias current that is delivered by this circuit which ultimately determines the bias level of the Output Buffers. A simplified schematic of the Buffer Bias circuit is shown in Figure 3. The buffer bias currents are generated with a $\Delta V_{BE}/R$ current regulator to generate a supply independent bias current to the Output Buffers.

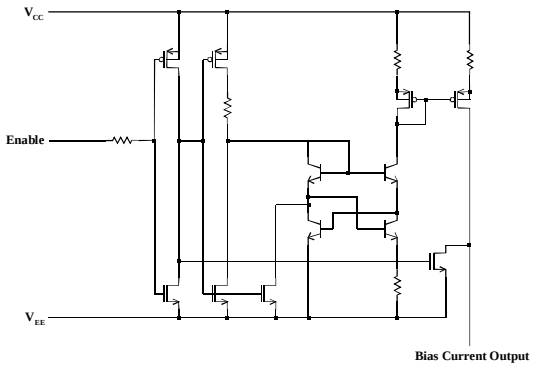


Figure 3. Simplified circuit diagram of the supply independent current regulator used in the Buffer Bias and Oscillator Bias.

### D. Output Buffers

The Output Buffers provide a programmable output power from the VCO IC. They are capable of delivering up to +6dBm of output power to a matched 50Ω load impedance. These outputs are high current open collector devices and require an external bias inductor and matching network.

### E. Oscillator Bias

The Oscillator Bias circuits are supply independent current regulators much like those of the Buffer Bias. These bias circuits provide the reference current for the Oscillators and are enabled and disabled by the logic inputs.

### F. Oscillators

The Oscillators are arranged in common collector Colpits configuration. These oscillators are configured with a novel phase noise reduction technique [2] to compensate for the reduced performance of the lower cost 0.4µm BiCMOS process.

A simplified schematic of the Oscillator is shown in Figure 4. This circuit is composed of the oscillating transistor (Q2) in a common collector configuration. A low frequency feedback circuit (Q1, C1, R1 and R2) serves to maintain the bias of the oscillating transistor Q2. A bias current is used to maintain the bias level and gain of the feedback circuit. The bias current of the oscillating transistor is set by means of an external resistor connected from the emitter to ground. Transistor Q1 sets the bias voltage on the base of Q2 such that enough voltage is generated across the external bias resistor to set the base voltage on Q1, this in turn allows Q1 to sink the current from the bias current source. The entire circuit is disabled when the bias current is shut off.

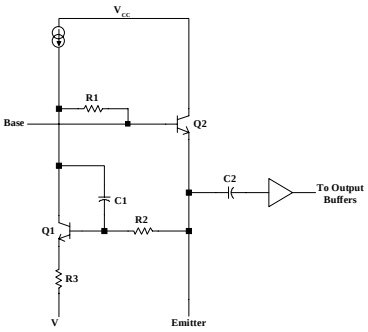


Figure 4. Simplified circuit diagram of the Oscillator

## G. Oscillator Buffers

The Oscillators have emitter coupled Oscillator Buffers to provide added isolation between the oscillator and the Output Buffers and are used as a means of commonly coupling the outputs of the Oscillators together.

## V. APPLICATION

A typical tank circuit and interface circuit is shown in Figure 5 and Figure 6 respectively. Figure 7 shows a typical VCO IC application circuit used in a triple band, dual mode application.

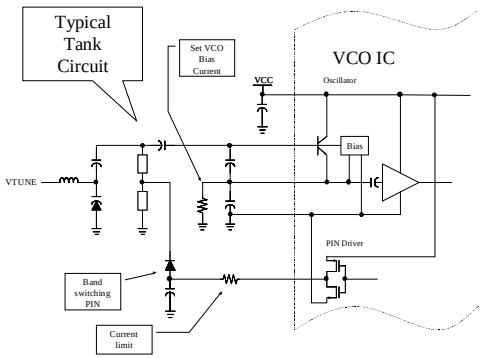


Figure 5. Simplified circuit diagram of a typical tank circuit and its interface into the VCO IC.

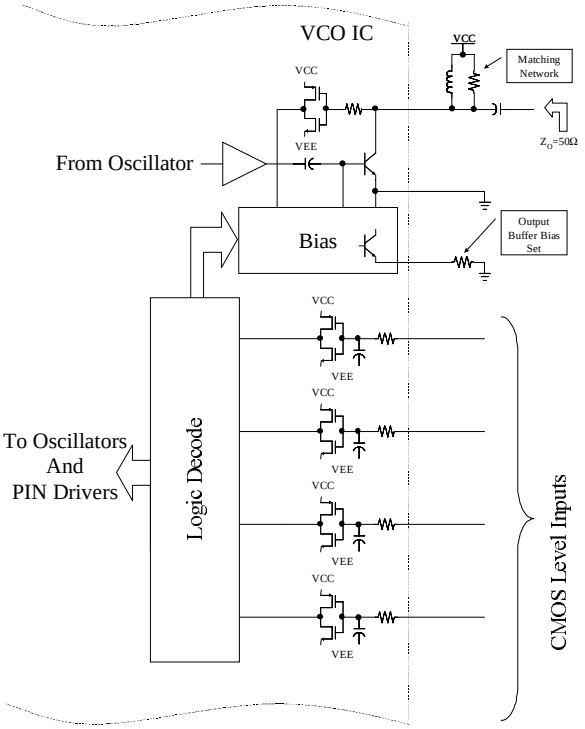


Figure 6. Simplified circuit diagram of a typical output and logic interface into the VCO IC.

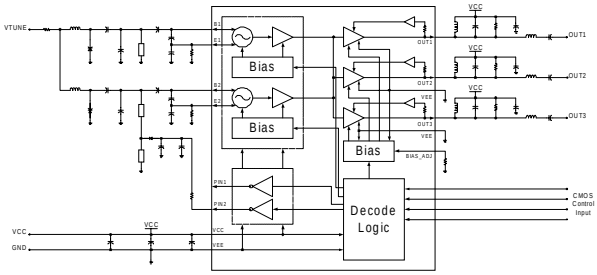


Figure 7. Typical Triple Band, Dual Mode application example of the VCO IC.

## VI. EXPERIMENTAL RESULTS

Measured phase noise performance is shown in Table 1. The VCO was phased locked and the phase noise was measured using a HP8562 Spectrum Analyzer (with phase noise option). Due to dynamic range limitation, as shown in Figure 8, the spectrum analyzer limits the phase noise measurement with offsets of greater than 1 MHz. The 20 MHz offset was measured by using external amplifiers to boost the dynamic range of the

spectrum analyzer.

| Frequency Offset | Phase Noise (dBc/Hz) |
|---|---|
| 100Hz | -40 |
| 1kHz | -65 |
| 10kHz | -90 |
| 100kHz | -110 |
| 1MHz | -134 |
| 20MHz | -162 |

Table 1. Phase noise performance at 900MHz ($P_{OUT}$ = +10dBm)

## VII. CONCLUSIONS

This paper has demonstrated the design and application of a very flexible VCO IC that is able to provide exceptional phase noise performance without relying on more expensive process technologies. Exceptional far out phase noise with an LC based resonator have been demonstrated. This shows that the VCO IC is capable of operating as a direct modulated oscillator in low cost GSM applications.

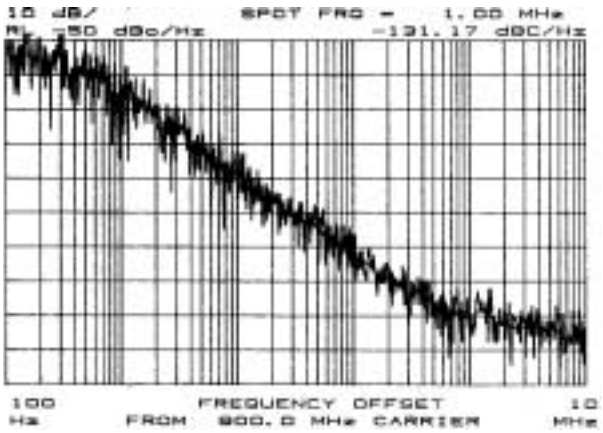


Figure 8. Phase noise plot (without dynamic range boost amplifier) at 900MHz ($P_{OUT}$ = +10dBm)

## VIII. REFERENCES


[1] Vida Ilderem, S. Bigelow, R. Braithwaite, F. Chai, P. Dahl, V. DelaTorre, S. Hildreth, C. Jasper, J. John, M. Kaneshiro, T. Keller, C. Kyono, I-S Lim, C. Moorer, K. Moore, C. Ramiah, J. Steele, J. Teplik, S. Wipf, Y. Yang, H. Zhao, D. Zupac, "RFBiCMOS Process Technologies at Motorola," IEEE Radio Frequency Integrated Circuits Symposium Workshop on Silicon/Silicon Germanium BiCMOS Processes and Circuit Techniques for RFICs, 2000.

[2] U.L. Rohde, "Phase Noise Improvements of Integrated Millimeterwave Oscillators," *5th International Workshop on International Non-Linear Microwave and Millimeterwave Circuits*, Gerhard-Mercator University, Duisburg, Germany, October 1998.